VeriSim

PRIMARIUS

Advanced Logic Simulator

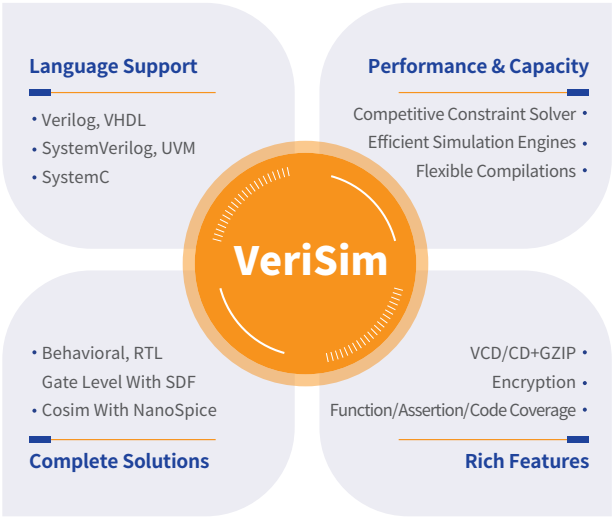
Introduction

VeriSim is an advanced logic simulator that offers a comprehensive digital design verification solution. Equipped with high-performance simulation engines and constraint solvers, it enhances compile time efficiency for large SoC designs.

VeriSim supports a wide array of languages, including Verilog, VHDL, SystemVerilog, SystemC, and their combinations. Its seamless integration of the Universal Verification Methodology (UVM) enables rapid verification testbench setup.

VeriSim provides extensive features for function, assertion, and code coverage testing. Its assertion-based verification feature facilitates the early detection and rectification of potential design flaws, thereby compressing the verification timeline and expediting the time-to-market for the product, with added security through encryption algorithms to safeguard customer IP.

By integrating with transistor-level NanoSpice simulators, VeriSim provides complete mixed signal verification solutions that cover the entire range of digital circuits, spanning from behavioral and RTL to gate-level designs.



Key Advantages

- High performance and capacity
  Innovated optimization from compilation, simulation to constraint solver engines
- Advanced simulation technology
  X-state propagation and race condition elimination
- Compatibility and usability
  Easy to use and quick migration from existing tools
- Extensive computing architecture
  Supports both X86 and ARM platforms
- One-stop mixed signal verification solution
  Native integration with NanoSpice for mixed signal verification

Specifications

- Languages supported
  - Verilog: 1995/2001/2005
  - SystemVerilog (SV): 2005/2009/2012/2017
  - VHDL: ieee87/ieee93/ieee08
  - SystemC
- Simulations supported
  - Verilog/SystemVerilog design
  - VHDL design
  - Verilog/SystemVerilog with SystemC design
  - Mixed design for both instantiating Verilog inside VHDL and instantiating VHDL inside Verilog
- Supports constraint solvers
- Supports function, assertion, and code coverage
- Supports waveform dumping
- Supports UVM-1.1b, UVM-1.1d and UVM-1.2
- Supports gate level with Standard Delay Format (SDF)
- Supports IEEE 1735 Encryption

Application Examples

- Testbench setup in system verification
- SystemVerilog and SystemC mixed language testbench
- Mixed signal SoC full chip verification by integrating NanoSpice
- Digital circuits from behavioral modeling, RTL to gate level with SDF