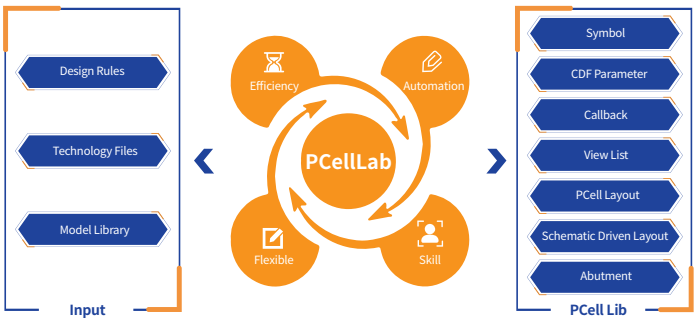
# PCellLab

PRIMARIUS

## Parameterized Cell Library Development Platform

## Introduction

In analog circuit design, the parameterized cell library (PCell) as an important component of the PDK (semiconductor process design kit) has become an indispensable part of the entire design process. With the rapid development of semiconductor technology, the increasingly complex structure of advanced semiconductor devices makes the development process of PCell more challenging. As an automated development platform for PCell, PCellLab has complete PCell development functions and advanced technology. PCell code can be automatically generated according to the process and design parameters inputted by users. It also reserves open interfaces for special processes and special needs so that users can customize input templates according to their own process characteristics, supporting PDK developers to complete development efficiently with high quality.




## Key Advantages

Versatility: Support bulk silicon planar process, SOI process, BCD process, FinFET process, etc.

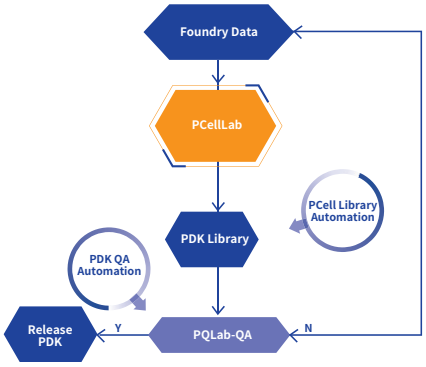
Completeness: Support automatic generation of PCell components such as Symbol, CDF, Callback, View, etc.

Automation: Highly integrated automated development process

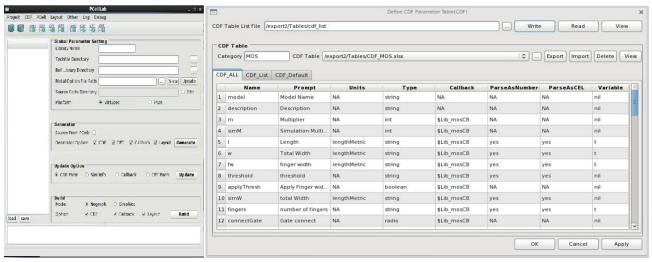
Efficiency: Rich and comprehensive PCell development functions significantly improve development efficiency.

Flexibility: Combination of standardized functions and customized functions to support user customization.

Easy to use: Friendly GUI supports mathematical expressions input, greatly shortening development learning curve and reducing development difficulty.




## Specifications



Support PCell automatic generation:

- Use simple and flexible GUI to input data, intelligently generate CDF files in PCell, Design Rule related information, Callback functions and layout code, etc.

Support multi-mode PCell Library compilation:

- Support CDF, Callback, layout independent or multiple simultaneous build mode
- Support single or multi-layer Metal Option at the same time

Support update function:

- Flexible update of single or multiple PCell CDF parameter information, simulation information, Design rule, Callback and other information, and automatically extract the differences

Support customized functions:

- Support automatic loading of customized functions

Supports creation of hierarchy structure:

- Support compilation of simple circuit-level hierarchy structure

## Applications

- Foundry PCell development
- Fabless/IP vendor PCell development

## Application Examples

Automatically generate layout from circuit schematic