NavisPro

PRIMARIUS

Hierarchical SoC Design Planning Solution

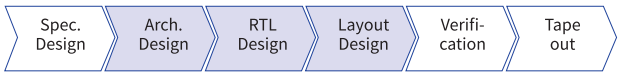
Introduction

NavisPro is a comprehensive design planning solution for chip estimation and floorplanning in RTL design, which enables the designers to predict and prevent physical implementation issues in the early floorplanning stage.

The RTL floorplanning is the first step of the physical implementation process in SoC design. NavisPro supports both top-down and bottom-up design methodologies, which are the same as the traditional sub-chip partitioning and chip-level integration process.

The hierarchical floorplanning feature resolves the complexity problem of SoC design. NavisPro supports interactive physical hierarchical partitioning and automatic pin placements of each sub-system, which is a critical constraint of sub-system layout, determining the extent of full-chip routing congestion.

Accurate estimation of the bus interconnect timing between sub-systems is critical for timing closure. NavisPro provides hierarchical net tracing capability across the design hierarchy. Estimating the interface net timing across the design hierarchy is essential for chip-level timing estimation.



Key Advantages

- Industry-proven SoC design planning solution
- Mixed-level design planning (RTL/Gate/Black-box)
- Flexible design abstraction management
- Rich sets of key engineering features
- Automatic block pin assignment and bus interconnect planning
- Standalone RTL design planning solution
- Minimum efforts for input data preparation
- Reduce design TAT by minimization of design iterations

Specifications

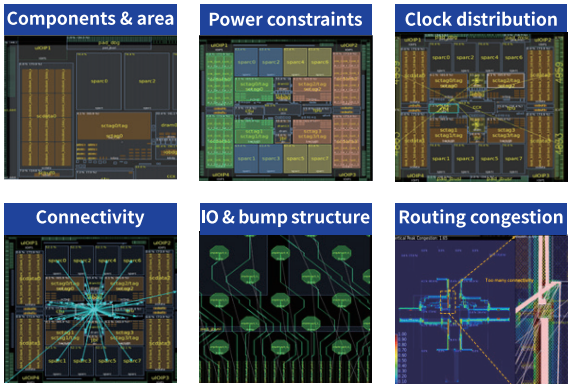
- Constraints driven RTL floorplanning
  - Bump array structuring
  - Bus interconnect exploration
  - Interconnect delay estimation
  - Automatic pipeline register placement
  - Global routing congestion analysis
  - Automatic & manual pin assignment
  - Block placement/shaping & chip area estimation
- Design & constraints exploration
  - RTL design exploration
  - Clock structure exploration
  - Low power intent exploration
- Flexible top-down & bottom-up floorplanning

Applications

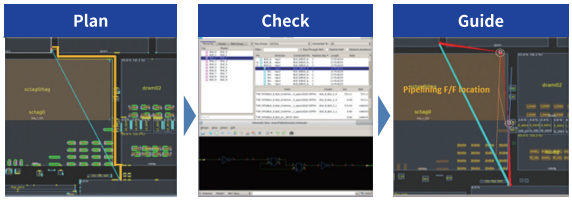
- RTL chip estimation
- RTL floorplanning

Application Examples

Constraint driven floorplanning



Bus interconnect planning



Hierarchical floorplanning